REMARKS

This paper is responsive to the Non-Final Office Action dated February 23, 2005. Claims 1-38 were examined. Claims 1-38 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,483,349 to Sakata et al.

Regarding claim 1, Applicants respectfully maintain that Sakata, alone or in combination with other references of record, fails to teach or suggest

> the sense amplifier equalization control signal having a rising transition effectively earlier than the rising transition of the sense amplifier enable signal, the sense amplifier enable signal having a falling transition effectively earlier than the falling transition of the sense amplifier equalization control signal, and the sense amplifier equalization signal being discharged into the sense amplifier enable signal,

as recited by claim 1. The Office Action relies on FIG. 2 of Sakata to supply this teaching. This portion of Sakata teaches a differential amplifier coupled to a voltage generating circuit (VTBG) to receive PIN and NIN (FIG. 2). Sakata teaches that:

> when the input signal varies over a range between VHmin and VLmax, the node PIN is fixed to the low level, the node NIN is fixed to the high level, and the MOSFETs Q2 and Q1 are maintained turned on. Therefore, an operation current formed by the constant-current MOSFET Q7 flows into the differential amplifier circuit to amplify the input signal VIN to form an output signal VOUT.

(Col. 8. lines 6-12). Sakata teaches further that

> the differential amplifier circuit effects the amplification operation at all times due to the constant current formed by the current source MOSFET Q7. Therefore, when the input signal VIN is larger than the reference voltage VREF, the output signal OUT is set to the high level and when the input signal VIN is lower than the reference voltage VREF, the output signal OUT is set to the low level.

(Col. 8, lines 28-35, emphasis added). The circuit of Sakata is amplifying at all times.

In contrast, the specification states at page 5, paragraph 1017 that "signal PR_L is an active-low signal that substantially turns on and substantially turns off a precharge operation in sense amplifier 106 and SE_H is an active-high signal that substantially turns on and substantially turns off the evaluation operation of sense amplifier 106." The specification at page 1, paragraph 1003, describes the equalization operation as being a state during which SE is "used to equalize sense amplifier nodes for a period that allows differential bit-lines to develop sufficient voltage differential to support sensing. Once the differential bit-lines have developed sufficient differential, SE is transitioned to cause the sense amplifier to actually sense the developed differential," during the evaluation operation. Nowhere does Sakata teach or suggest equalization, as required by claim 1.

Thus, Sakata fails to teach or suggest the sense amplifier equalization control signal having a rising transition effectively earlier than the rising transition of the sense amplifier enable signal, the sense amplifier enable signal having a falling transition effectively earlier than the falling transition of the sense amplifier equalization control signal, and the sense amplifier equalization signal being discharged into the sense amplifier enable signal, as required by claim 1. For these reasons, Applicants respectfully maintain that claim 1 distinguishes over Sakata and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon, be withdrawn.

Regarding claim 5, Applicants respectfully maintain that Sakata, alone or in combination with other references of record, fails to teach or suggest

> a sense amplifier equalization enable node for receiving a first signal and a sense amplifier evaluation enable node for receiving a second signal, the nodes coupled to the impedance and respective ones of the first and second switches, wherein a first transition of the first signal is effectively earlier than a first transition of the second signal and a second transition of the second signal is effectively earlier than a second transition of the first signal,

as recited by claim 5. The Office Action relies on FIG. 2 of Sakata to supply this teaching. This portion of Sakata teaches a differential amplifier coupled to a voltage generating circuit (VTBG) to receive PIN and NIN (FIG. 2). Sakata teaches that:

> when the input signal varies over a range between VHmin and VLmax, the node PIN is fixed to the low level, the node NIN is fixed to the high level, and the MOSFETs Q2 and Q1 are maintained turned on. Therefore, an operation current formed by the constant-current MOSFET Q7 flows into the differential amplifier circuit to amplify the input signal VIN to form an output signal VOUT.

(Col. 8. lines 6-12). Sakata teaches further that

> the differential amplifier circuit effects the amplification operation at all times due to the constant current formed by the current source MOSFET Q7. Therefore, when the input signal VIN is larger than the reference voltage VREF, the output signal OUT is set to the high level and when the input signal VIN is lower than the reference voltage VREF, the output signal OUT is set to the low level.

(Col. 8, lines 28-35, emphasis added). The circuit of Sakata is amplifying at all times.

In contrast, the specification states at page 5, paragraph 1017 that "signal PR_L is an active-low signal that substantially turns on and substantially turns off a precharge operation in sense amplifier 106 and SE_H is an active-high signal that substantially turns on and substantially turns off the evaluation operation of sense amplifier 106." The specification at page 1, paragraph 1003, describes the equalization operation as being a state during which SE is "used to equalize sense amplifier nodes for a period that allows differential bit-lines to develop sufficient voltage differential to support sensing. Once the differential bit-lines have developed sufficient differential, SE is transitioned to cause the sense amplifier to actually sense the developed differential," during the evaluation operation. Nowhere does Sakata teach or suggest an equalization enable node, as required by claim 5.

Thus, Sakata fails to teach or suggest a sense amplifier equalization enable node for receiving a first signal and a sense amplifier evaluation enable node for receiving a second signal, the nodes coupled to the impedance and respective ones of the first and second switches, wherein a first transition of the first signal is effectively earlier than a first transition of the second signal and a second transition of the second signal is effectively earlier than a second transition of the first signal, as required by claim 5. For these reasons, Applicants respectfully

maintain that claim 5 distinguishes over Sakata and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 5 and all claims dependent thereon, be withdrawn.

Regarding claim 23, Applicants respectfully maintain that Sakata, alone or in combination with other references of record, fails to teach or suggest

> substantially turning off equalization of the sense amplifier before substantially turning on a sensing operation and effectively turning off the sensing operation before effectively turning on the equalization of the sense amplifier,

as recited by claim 23. The Office Action relies on FIG. 2 of Sakata to supply this teaching. This portion of Sakata teaches a differential amplifier coupled to a voltage generating circuit (VTBG) to receive PIN and NIN (FIG. 2). Sakata teaches that:

> when the input signal varies over a range between VHmin and VLmax, the node PIN is fixed to the low level, the node NIN is fixed to the high level, and the MOSFETs Q2 and Q1 are maintained turned on. Therefore, an operation current formed by the constant-current MOSFET Q7 flows into the differential amplifier circuit to amplify the input signal VIN to form an output signal VOUT.

(Col. 8. lines 6-12). Sakata teaches further that

> the differential amplifier circuit effects the amplification operation at all times due to the constant current formed by the current source MOSFET Q7. Therefore, when the input signal VIN is larger than the reference voltage VREF, the output signal OUT is set to the high level and when the input signal VIN is lower than the reference voltage VREF, the output signal OUT is set to the low level.

(Col. 8, lines 28-35, emphasis added). The circuit of Sakata is amplifying at all times.

In contrast, the specification states at page 5, paragraph 1017 that "signal PR_L is an active-low signal that substantially turns on and substantially turns off a precharge operation in sense amplifier 106 and SE_H is an active-high signal that substantially turns on and substantially turns off the evaluation operation of sense amplifier 106." The specification at page 1, paragraph 1003, describes the equalization operation as being a state during which SE is

"used to equalize sense amplifier nodes for a period that allows differential bit-lines to develop sufficient voltage differential to support sensing. Once the differential bit-lines have developed sufficient differential, SE is transitioned to cause the sense amplifier to actually sense the developed differential," during the evaluation operation. Nowhere does Sakata teach or suggest equalization, as required by claim 23.

Thus, Sakata fails to teach or suggest substantially turning off equalization of the sense amplifier before substantially turning on a sensing operation and effectively turning off the sensing operation before effectively turning on the equalization of the sense amplifier, as required by claim 23. For these reasons, Applicants respectfully maintain that claim 23 distinguishes over Sakata and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 23 and all claims dependent thereon, be withdrawn.

Regarding claim 34, Applicants respectfully maintain that Sakata, alone or in combination with other references of record, fails to teach or suggest

> means for substantially turning off precharging of the sense amplifier before substantially turning on a sensing operation and means for substantially turning off the sensing operation before substantially turning on the precharging of the sense amplifier,

as recited by claim 34. The Office Action relies on FIG. 2 of Sakata to supply this teaching. This portion of Sakata teaches a differential amplifier coupled to a voltage generating circuit (VTBG) to receive PIN and NIN (FIG. 2). Sakata teaches that:

> when the input signal varies over a range between VHmin and VLmax, the node PIN is fixed to the low level, the node NIN is fixed to the high level, and the MOSFETs Q2 and Q1 are maintained turned on. Therefore, an operation current formed by the constant-current MOSFET Q7 flows into the differential amplifier circuit to amplify the input signal VIN to form an output signal VOUT.

(Col. 8. lines 6-12). Sakata teaches further that

> the differential amplifier circuit effects the amplification operation at all times due to the constant current formed by the current source MOSFET Q7. Therefore,

> when the input signal VIN is larger than the reference voltage VREF, the output signal OUT is set to the high level and when the input signal VIN is lower than the reference voltage VREF, the output signal OUT is set to the low level.

(Col. 8, lines 28-35, emphasis added). The circuit of Sakata is amplifying at all times.

In contrast, the specification states at page 5, paragraph 1017 that "signal PR_L is an active-low signal that substantially turns on and substantially turns off a precharge operation in sense amplifier 106 and SE_H is an active-high signal that substantially turns on and substantially turns off the evaluation operation of sense amplifier 106." The specification at page 1, paragraph 1003, describes the equalization operation as being a state during which SE is "used to equalize sense amplifier nodes for a period that allows differential bit-lines to develop sufficient voltage differential to support sensing. Once the differential bit-lines have developed sufficient differential, SE is transitioned to cause the sense amplifier to actually sense the developed differential," during the evaluation operation. Nowhere does Sakata teach or suggest precharging, as required by claim 34.

Thus, Sakata fails to teach or suggest means for substantially turning off precharging of the sense amplifier before substantially turning on a sensing operation and means for substantially turning off the sensing operation before substantially turning on the precharging of the sense amplifier, as required by claim 34. For these reasons, Applicants respectfully maintain that claim 34 distinguishes over Sakata and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 34 and all claims dependent thereon, be withdrawn.

Regarding claim 37, Applicants respectfully maintain that Sakata, alone or in combination with other references of record, fails to teach or suggest

> forming a sense amplifier equalization enable node for receiving a first signal and a sense amplifier evaluation enable node for receiving a second signal, the nodes coupled to the impedance and respective ones of the first and second switches, wherein a first transition of the first signal is effectively earlier

> than a first transition of the second signal and a second transition of the second signal is effectively earlier than a second transition of the first signal,

as recited by claim 37. The Office Action relies on FIG. 2 of Sakata to supply this teaching. This portion of Sakata teaches a differential amplifier coupled to a voltage generating circuit (VTBG) to receive PIN and NIN (FIG. 2). Sakata teaches that:

> when the input signal varies over a range between VHmin and VLmax, the node PIN is fixed to the low level, the node NIN is fixed to the high level, and the MOSFETs Q2 and Q1 are maintained turned on. Therefore, an operation current formed by the constant-current MOSFET Q7 flows into the differential amplifier circuit to amplify the input signal VIN to form an output signal VOUT.

(Col. 8. lines 6-12). Sakata teaches further that

> the differential amplifier circuit effects the amplification operation at all times due to the constant current formed by the current source MOSFET Q7. Therefore, when the input signal VIN is larger than the reference voltage VREF, the output signal OUT is set to the high level and when the input signal VIN is lower than the reference voltage VREF, the output signal OUT is set to the low level.

(Col. 8, lines 28-35, emphasis added). The circuit of Sakata is amplifying at all times.

In contrast, the specification states at page 5, paragraph 1017 that "signal PR_L is an active-low signal that substantially turns on and substantially turns off a precharge operation in sense amplifier 106 and SE_H is an active-high signal that substantially turns on and substantially turns off the evaluation operation of sense amplifier 106." The specification at page 1, paragraph 1003, describes the equalization operation as being a state during which SE is "used to equalize sense amplifier nodes for a period that allows differential bit-lines to develop sufficient voltage differential to support sensing. Once the differential bit-lines have developed sufficient differential, SE is transitioned to cause the sense amplifier to actually sense the developed differential," during the evaluation operation. Nowhere does Sakata teach or suggest equalization, as required by claim 37.

Thus, Sakata fails to teach or suggest forming a sense amplifier equalization enable node for receiving a first signal and a sense amplifier evaluation enable node for receiving a second

signal, the nodes coupled to the impedance and respective ones of the first and second switches, wherein a first transition of the first signal is effectively earlier than a first transition of the second signal and a second transition of the second signal is effectively earlier than a second transition of the first signal, as required by claim 37. For these reasons, Applicants respectfully maintain that claim 37 distinguishes over Sakata and all references of record. Accordingly, Applicants respectfully request that the rejection of claim 37 and all claims dependent thereon, be withdrawn.

In summary, claims 1-38 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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